GA34-0244-0

File No. S1-09

IBM Series/1
Binary Synchronous
Communications Feature
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Preface

This publication describes the IBM Series/1 Binary Synchronous Communications Features. The reader should be an experienced Series/1 assembler-language programmer, who writes, maintains, and debugs machine-level-language programs. The reader should also be familiar with binary and hexadecimal numbering systems and stored-program concepts.

The subject matter is presented in two chapters and three appendices:

- Chapter 1 introduces the binary synchronous communications features.

- Chapter 2 describes the Series/1 machine-level language that the processor uses to transfer data to and from the attachment features and devices that connect to the communication line.

- Appendix A contains a summary of the commands, device control blocks (DCBs), cycle-steal status words, and condition codes associated with the binary synchronous communications features.

- Appendix B contains a test procedure for the operator to use to verify that the attachment feature is able to transmit and receive test data through a test cable.

- Appendix C contains a flow chart outlining the program steps that may be used to prepare the binary synchronous communications attachment features to process subsequent transmit and receive operations.

- Appendix D lists the control and data characters used by the binary synchronous communications features.

Prerequisite Publications

- *IBM Series/1 Principles of Operation*, GA34-0152.

- Refer to *IBM Series/1 Graphic Bibliography*, GA34-0055, for the name and order number of the appropriate feature description manual for your processor.

Related Publications

- *IBM Series/1 System Selection Guide*, GA34-0143

- *IBM Series/1 Customer Site Preparation Manual*, GA34-0050

- *IBM Series/1 Pocket Digest*, GX34-0104

Contents

Chapter 1. Introduction

This chapter provides an overview of the Series/1 Binary Synchronous Communications features:

- Binary Synchronous Communications Single-Line Control/medium speed
- Binary Synchronous Communications Single-Line Control/high speed
- Binary Synchronous Communications 8-Line Control and Binary Synchronous Communications 4-Line Adapter

The following communication characteristics apply to all BSC features:

- Data transmission is serial-by-bit, using the BSC method of transmission.
- The features communicate with terminals or host systems using Extended Binary Coded Decimal Interchange Code (EBCDIC) and American Standard Code for Information Interchange (ASCII).
- Bit rates of up to 9,600 bits per second (bps) on the medium-speed, single-line feature, and up to 56,000 bps on the high-speed, single-line feature.
- The features can be primary or secondary stations.
- The single-line features can IPL the Series/1 processor.
- Transparency (available when using EBCDIC) is standard.
- Intermediate block checking is standard.
- Internal clocking is selected by installing a jumper on the feature cards (medium-speed only).
- Answer-tone generation is selected by installing a jumper on the feature cards (medium-speed only).

Single-Line Control Feature/Medium Speed

The single-line control feature provides circuitry for one, half-duplex, medium-speed (up to 9,6000 bytes per second [bps]) line that can IPL the processor from a host system. This feature can be used as either a primary or secondary station.

Single-Line Control Feature/High Speed

The single-line, control/high speed feature provides circuitry for one, half-duplex, high-speed (up to 56,000 bps) line that can IPL the processor from a host system. This feature can be used as either a primary or secondary station with leased-line applications only.

Eight-Line Control and 4-Line Adapter Features

These features can control up to eight half-duplex communications lines at medium speeds. The maximum aggregate bit rate possible through the 8-line control feature is 33,600 bps. Multiple-line BSC features are not able to IPL from a host system. The BSC features allow a Series/1 processor to communicate with telecommunication equipment or other processors with compatible adapters.

Configurations

The BSC features are available in single-line and multiple-line configurations. The single-line configurations are contained on one card. The multiple-line configuration provides up to eight lines. The multiple-line configuration contains either two or three feature cards - two cards for one to four lines, three cards for five to eight lines.

When eight lines are installed, the multiple-line feature can handle up to 9,600 bps on lines 0 and 1, and up to 2,400 bps on all other lines. When four lines are installed, each line can run at speeds of up to 4,800 bps. The bit rate for an individual line is established by the modem's transmit and receive clocks. If the modem does not provide clocking on medium-speed attachments, internal clocking must be used. Internal clocking provides bit rates of 600 bps or 1,200 bps (under program control). The high-speed attachment makes no provision for internal clocking.

Note: When referring to the BSC Single-Line Control/medium speed or the BSC Single-Line Control/high speed, the term **single-line attachment** is used. When referring to the BSC 8-Line Control and one or two BSC 4-Line Adapters, the term **multiple-line attachment** is used. The single-line and multiple-line attachments operate in half-duplex mode.

Indicator panel connectors

Device address

XXXX X011
XXXX X010
XXXX X001
XXXX X000

Device address

XXXX X111
XXXX X110
XXXX X101
XXXX X100

Binary synchronous communication single-line control
or
Binary synchronous communication single-line control—high speed

Binary synchronous communication 4-line adapter

Binary synchronous communication 8-line control

Binary synchronous communication 4-line adapter

*Modem interface connectors

Note: XXXX = base device address

Binary Synchronous Communications Control Feature

Interfaces

In all features described in this book, except the high-speed BSC an EIA[1]RS232-C and CCITT[2] V.24 interface is provided for each line. The interface directly drives or ends an external modem. The high-speed BSC provides interfaces compatible with the Western Electric 303 data set (or equivalent) and CCITT recommendation V.35.

The attachments can communicate with remote stations over private lines, leased common-carrier facilities, or switched voice-grade common-carrier lines, or they can be directly connected to remote stations.

Some modems disconnect automatically when the communication feature's DTR signal is deactivated. To deactivate this signal, issue a Start command with a disable operation specified in the device control block, or use the communications indicator panel.

Data Links

Each communication line operates with one of the following types of data links:

- Point-to-point nonswitched
- Point-to-point switched
- Multipoint nonswitched
- Direct connect

Point-to-Point Nonswitched

A point-to-point nonswitched data link consists of a local station connected to a single remote station. Such a line is referred to as nonswitched because there is a permanent connection between the local station and the remote station through their respective modems.

```
+---------+        +---------+              +---------+        +---------+
| Local   |        |         |              |         |        | Remote  |
| station |--------| Modem   |--------------| Modem   |--------| station |
|         |        |         |              |         |        |         |
+---------+        +---------+              +---------+        +---------+
```

---

[1]   Electronic Industries Association
[2]   The International Telegraph and Telephone Consultative Committee.

Point-to-Point Switched

A point-to-point switched data link consists of a local station connected to one of several remote stations after a link has been established between the local station and the remote station. The connection is maintained only for the duration of the communication.
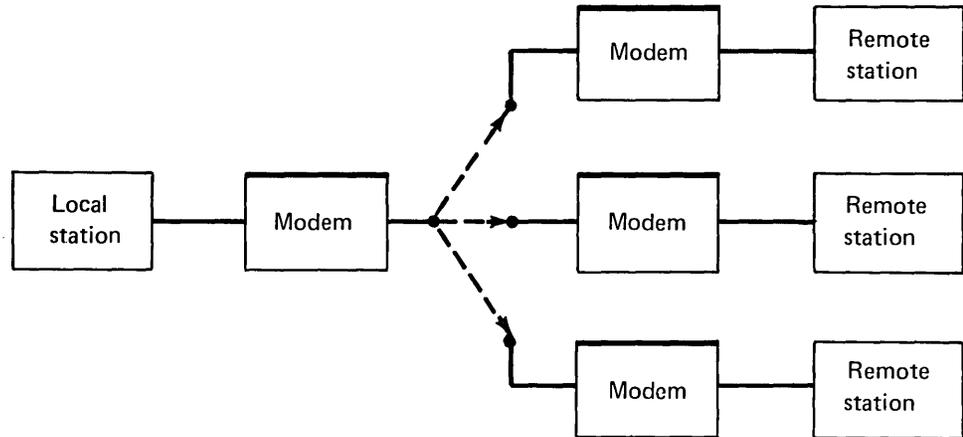
Multipoint Nonswitched

A multipoint nonswitched data link consists of a primary station connected to several secondary stations through their respective modems. The primary station polls the secondary stations, using unique station addresses. Only the addressed station can respond to the poll.
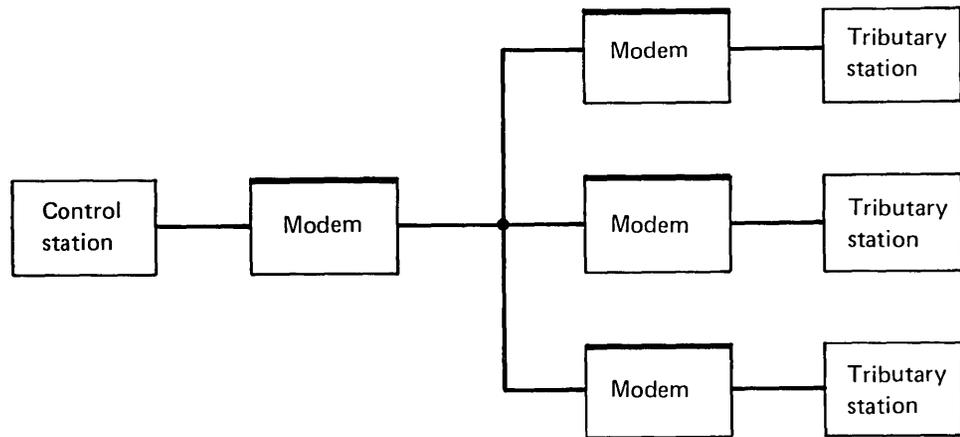
Direct Connect

A direct-connect data link consists of two stations directly connected.
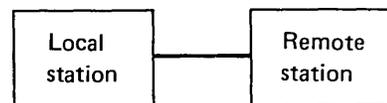
Establishing a Switched-Line Data Link

Initiating a Call

1. Load the program and make sure that the DTR signal is active.
2. Place the modem in talk mode.
3. Dial the remote station. The operator of the remote station will answer your call, or you will hear a high-pitched tone indicating that the remote modem is in auto-answer mode. If you talk to the operator, request that the remote modem be placed in data mode (or equivalent.)
4. Place your modem in data mode (or equivalent) and hang up the receiver.

Answering a Call

1. When you are called, lift the receiver and talk to the operator of the other system.
2. Make sure that the program is loaded and the DTR signal is active.
3. Put your modem in data mode (or equivalent) before the caller puts the calling modem in data mode, and hang up the receiver.

Chapter 2. Operations

Operating Modes

The attachment has the following operating modes that are selected by control characters:

- Text
- Transparent text
- Control
- Selected
- Passive

Text

Text mode is selected when the first start-of-heading (SOH) or start-of-text (STX) control character is decoded. Subsequent SOH and STX characters are treated as data characters. During text mode, the attachment processes header or text characters and accumulates a block check character (BCC). Synchronization (SYN) characters and the first SOH or STX characters decoded are not included in the BCC accumulation. Text mode is ended after an end-of-text (ETX) or end-of-transmission-block (ETB) character is decoded by the attachment.

Transparent Text

Transparent text mode is selected when a data-link-escape (DLE) STX sequence is decoded during a transmit or receive operation. While in this mode, any kind of binary data can be transmitted or received. The following changes from text mode occur:

- The attachment recognizes individual control characters or control sequences, (such as ETB, STX, and enquiry [ENQ]), only as data, with no other associated function.
- All inserted SYN characters are preceded automatically by a DLE character (DLE-SYN).
- A second DLE is attached automatically to every data DLE to distinguish it as a DLE control character, rather than data. This second DLE of the Data DLE sequence and all DLE SYN sequences are automatically deleted upon reception and do not enter main storage.

To exit transparent text mode, one of the following ending sequences are required:

- DLE-ETX
- DLE-ETB
- DLE-ITB
- DLE-ENQ

These sequences must be transmitted by using the exit transparent operation (bit 14 of the control word in the DCB is set to 1.) In transparent text mode, the transmitting attachment automatically inserts a second DLE between the first DLE and the ETX, ETB, ENQ, or ITB. The receiving station discards the first DLE. The inserted DLE and the ETX, ETB, ENQ, or ITB are considered as two data characters and placed in storage. The exit transparent operation prevents the attachment from inserting a second DLE. The receiving station recognizes the ending sequences as such, not data when the exit transparency operation is used (bit 14 of the DCB set to 1). Then the DLEs in these ending sequences are true DLEs and are not placed in storage at the receiver, they should not be included in the byte count for the receiving station.

Only DLE-ITB leaves the attachment in text mode; all the others cause a COD.

During transparent text mode, a BCC is accumulated as in normal text mode. The only DLE characters included in the BCC are the data DLEs.

Control Mode

In a multipoint configuration, when the attachment receives a valid EOT sequence, it enters control mode. While in control mode, the attachment monitors for its station address. If the attachment does not enter selected mode and detects an address sequence other than its own, character synchronization is reset.

The multiple-line attachment must be in receive mode to recognize the EOT character. Due to its IPL capability, the single-line attachment monitors the line for an EOT character while it is in control mode (that is, no command pending). An EOT character following the leading SYN-SYN sequence places the single-line attachment in control mode.

Selected Mode

The attachment enters selected mode when it decodes its station address twice (contiguously) after establishing byte synchronization. If a receive operation has been initiated, the message sequence, starting with the second station address character, is transferred to storage.

Note: The attachment's station address (used in multipoint configuration only) is determined by discrete jumpers on the feature card. Control characters may not be used as an address. The bit-2 position in storage (station address) cannot be wired. In EBCDIC, this is bit 2; in ASCII, this is bit 6. The program may use these bits to differentiate between a polling and a selecting sequence.

Multipoint address bit 0 must not be set to 1 on when using ASCII.

Passive Mode

The attachment in a multipoint network is in passive mode when it is not in selected or in control mode. Passive mode is entered when the attachment is powered on. The attachment enters other modes, depending upon the characters recived on the line, as previously described.

IPL Mode

Initial program load (IPL) by a host system may be accomplished through a **single-line** attachment using EBCDIC characters only. A jumper (for bit 0 of the multipoint address) must be installed on the feature card to allow the attachment to IPL the processor.

If an IPL sequence (DC1-DC1-ENQ) is received, the attachment responds with an EBCDIC acknowledgment (ACK0) after a 50-millisecond delay.

If the attachment is a multipoint tributary station, its address must be included in the IPL sequence, as shown in the following example. (It must also have been placed in control mode as described earlier).

```
Host
system                                          Series/1

SYN     ────────────▶
SYN     ────────────▶
(Addr)* ────────────▶
(Addr)* ────────────▶
DC1     ────────────▶
DC1     ────────────▶
ENQ     ────────────▶
              ◀──────────── ACK0 (hardware)    Machine reset
DLE     ────────────▶
STX     ────────────▶


IPL
message ─────────────▶



DLE     ────────────▶
ETX     ────────────▶                          Begin execution
                                                on level 0 at
                                                address 000

        ◀──────────── ACK0/1 (software)        Program transmits ACK1
                                                to acknowledge host system
```
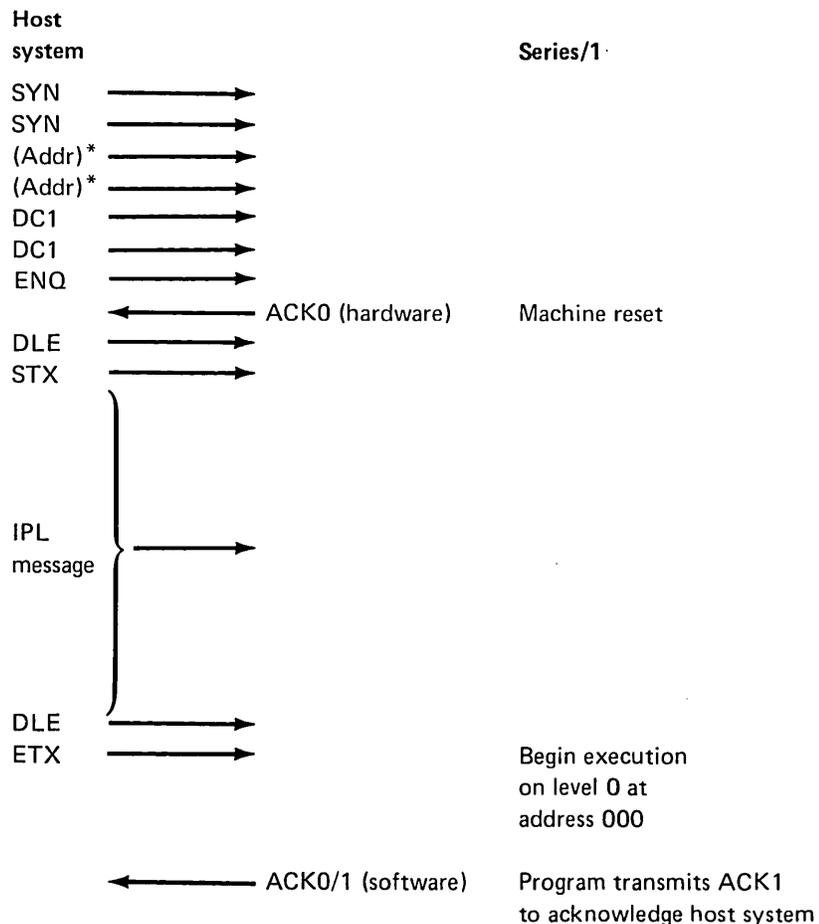
*Used only if the attachment
is a multipoint tributary.

The host must then transmit DLE-STX (to enter transparent text mode) followed by the IPL program. This sequence (DLE-STX) is not checked by the attachment

for validity and is not placed into storage. The attachment enters transparent text mode and places all following data into storage beginning at location 0000.

Upon receiving a DLE-ETX followed by a valid BCC, the attachment presents a device-end interrupt request, on level 0, with the device address in register 7. The IPL program must handle this interrupt request and must also transmit a positive acknowledgement back to the host system.

If the IPL operation is unsuccessful, the attachment holds the processor in IPL mode (Load light is on) and monitors the line for a retry of the IPL operation. A general logic flow for a switched-line IPL sequence follows.

Enter

(1)

Ring signal — No

Yes

Attachment sets DTR on

Transmit answer-tone, if required

Present attention interrupt

Interrupt accepted — No

Yes

Attachment delay for 50 msec

Operate I/O request — No

Yes

Attachment does as instructed

Line monitored for 13 seconds for IPL sequence (or retry)

Sequence seen — No

Yes

Reset processor

Attachment returns ACK0

IPL program placed into storage

Attachment disconnects (drops DTR)*

(1)

'Yes

BCC error

No

Interrupt on level 0 with device address in register 7; restart processor (address 0000)

General logic flow for switched-line IPL sequence

Notes:

1. To IPL an unattended processor on a switched network, the modem must be capable of automatically answering calls. If the line is not enabled (data terminal ready made active) and the allow-IPL and switched-line jumpers are installed, the attachment activates data terminal ready and presents an attention interrupt request upon detecting the ring signal. If the processor does not issue a command or if the attention interrupt is not accepted, the attachment monitors the line for approximately 13 seconds for an IPL sequence. (Any

command the processor gives during this period is accepted.) The line is disconnected (DTR deactivated) if no IPL sequence is detected within this time period. If the line was enabled before to this sequence, the DTR line stays active.

2. On a leased line, the attachment cannot receive an IPL unless DTR is set to 1.

3. Some modems do not supply clocking and cannot run at speeds higher than 600 bps. These modems require the use of the internal clocking feature of the BSC attachments. Internal clocking supplies clocking at 1,200 bps. The 600-bps rate of internal clocking can only be selected by a program already in storage; therefore, the system cannot be IPLed by the BSC attachments when such a modem is used.

4. The maximum number of bytes that the host IPL program can load is 65,535; however, the quality of the transmission line must be considered when transmitting 65,535 bytes.

Transmission Codes

The BSC attachments allow data communication using EBCDIC or ASCII line codes. ASCII can be specified by the program after the IPL. The attachment establishes EBCDIC if:

• No code is specified

• A power-on reset occurs

• A system reset occurs

Note: The EBCDIC and ASCII character assignments are shown in Appendix D.

Control Characters

The BSC control characters and sequences follow.

Name	Mnemonic	EBCDIC	ASCII
Start of heading	SOH	SOH	SOH
Start of text	STX	STX	STX
End of transmission block (Note 1)	ETB	ETB	ETB
End of text (Note) 1)	ETX	ETX	ETX
End of transmission (Note 1)	EOT	EOT	EOT
Enquiry (Note 1)	ENQ	ENQ	ENQ
Negative acknowledge (Note 1)	NAK	NAK	NAK
Synchronous idle	SYN	SYN	SYN
Data link escape	DLE	DLE	DLE
Immediate block character	ITB	IUS	US
Initial program load (Note 2)	IPL	DC1 DC1 ENQ	
Even acknowledge (Note 1)	ACK0	DLE(70)	DLE0
Odd acknowledge	ACK1	DLE/	DLE1
Wait before transmit-positive acknowledge (Note 1)	WACK	DLE,	DLE;
Mandatory disconnect (Note 1)	DISC	DLE EOT	DLE EOT
Reverse interrupt (Note 1)	RVI	DLE@	DLE<
Temporary text delay	TTD	STX ENQ	STX ENQ
Transparent start of text (Note 3)	XSTX	DLE STX	
Transparent intermediate block (Note 3)	XITB	DLE IUS	
Transparent end of text (Note 3)	XETX	DLE ETX	
Transparent end of transmission block (Note 3)	XETB	DLE ETB	
Transparent synchronous idle (Note 3)	XSYN	DLE SYN	
Transparent block cancel (Note 3)	XENQ	DLE ENQ	
Transparent TTD (Note 3)	XTTD	DLE STX DLE ENQ	
Data DLE in transparent mode (Note 3)	XDLE	DLE DLE	

Notes:

1. These control characters and sequences cause a change-of-direction (COD) interrupt request after the required action completes.
2. Not applicable in ASCII format.
3. Transparent mode not available in ASCII.

The functions of the control characters follow:

Mnemonic	Function
SOH or STX	Resets control mode and sets the adapter to text mode. BCC accumulation starts with the first character after the first SOH or STX character is transmitted/received.
ETB or ETX	Reset text mode with BCC comparison.
EOT	End of transmission.
ENQ	Reset text mode without BCC transmission and comparison.
NAK	Negative response to a request for a reply, or to a block of heading, or a block of text in error.
SYN	Transmitted automatically by the adapter to establish and maintain synchronization.
DLE	Alert the adapter to test the next character for a defined control sequence in transparent text mode. In nontransparent text mode, DLE is treated as data.
ITB	Included in the BCC; it causes the BCC to be sent.
IPL	Initiate an IPL sequence.
ACK0	Affirmative acknowledgement of even blocks.
ACK1	Affirmative acknowledgement of odd blocks.
WACK	A temporary not-ready-to-continue (or not-ready-to-receive) condition.
DISC	Used only on switched communication facilities to initiate a disconnect.
RVI	Reverses direction of data transfer.
TTD	Alerts the receiving station of a temporary text delay
XSTX	Switches off control mode and sets the adapter to transparent text mode.
XITB	Same as ITB, but switches off transparent text mode.
XETX/XETB	Same as ETB or ETX, but switches off transparent mode.
XSYN	Transmitted automatically by the adapter to establish and maintain synchronization in transparent text mode.
XENQ	Switches off transparent text mode and cancel the current block of data.
XTTD	Alerts the receiving station to a temporary text delay in transparent text mode.
XDLE	In transparent text mode, the transmitter adds a second DLE after each data DLE. At the receiver, the first DLE is removed and does not enter storage or the BCC.

Data Flow

Transmit

Transmission data is fetched from storage two characters at a time unless the byte count is equal to an odd value. The high-order byte holds the first character to be sent; the low-order byte holds the next character. After a character has been transferred into the serializer/deserializer (SERDES), it is transmitted over the line, low-order bit first.

ASCII characters in storage are eight bits long, seven data bits plus one parity bit. This parity bit should not be confused with the parity bit in storage. The ASCII parity bit is bit 0 in a byte of storage.

The attachment does not check ASCII parity during transmit operations; therefore, the program must maintain odd parity in storage bits 0–7 when using ASCII. The BSC attachment data flow is illustrated below.

Receive data → SERDES 0|1|2|3|4|5|6|7 → Transmit data

Buffer — Send/receive buffer

Storage data register

Storage	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
EBCDIC	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
ASCII	P	7	6	5	4	3	2	1	P	7	6	5	4	3	2	1

First character   Second character
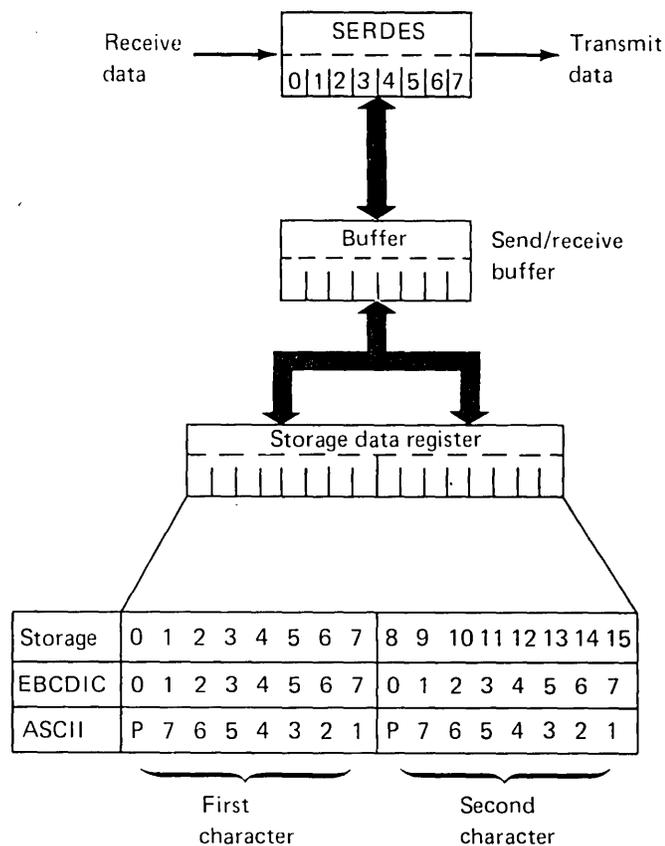
Receive

The first bit received is transferred into the low-order bit position of a byte, the second bit received is transferred into the next higher bit position, and so on until a character is assembled.

Two characters are assembled in the attachment before data is transferred to storage (except as noted above). When two characters are to be transferred to storage, the first character received is loaded into the high-order byte of the storage data register and the next character is loaded in the low-order byte before the data is transferred to storage. Data is written into main storage without any code translation.

Line Error Checking

Two different types of checking are employed, depending upon the code selected. Cyclic redundancy check (CRC) is used with EBCDIC and longitudinal redundancy and vertical redundancy checking (LRC/VRC) is used with ASCII.

Error correction is accomplished by retransmitting the data block that was in error.

Synchronization and Timing

The attachment receives strobe pulses from the modem; these pulses establish and maintain bit synchronization. If the modem does not supply a pulse, the internal clocking feature must be wired on to supply synchronization. Whichever form of bit synchronization is used, a specific series of characters precedes each transmission to establish character synchronization.

Transmit Synchronization

The attachment automatically begins transmission with a leading pad character (hex 55) followed by the initial synchronizing pattern of two SYN characters. If internal clocking is being used, the attachment transmits two leading pad characters.

To maintain synchronization, the attachment inserts a synchronization pattern of SYN-SYN at approximately one-second intervals. In transparent text mode this synchronization pattern is DLE-SYN. These characters are also inserted as time-fill characters when the attachment is not transmitting such as when it is fetching a new device control block (DCB) during a chaining operation.

SYN Insertion: SYN characters or transparent SYN characters are inserted automatically during transmission or between chaining. This is done to maintain synchronization.

SYN Deletion: SYN characters or transparent SYN characters are deleted and not placed in storage.

Trailing Pad Characters: The attachment automatically transmits a trailing pad character (hex FF) after every COD character or after the BCC if the change of direction calls for BCC. This ensures that the last character sent (COD or BCC) goes online in its entirety. A pad of hexadecimal FF also provides the second character of the NAK and EOT control character sequences. The attachment does not begin an interrupt request or chaining operation until the entire pad character is transmitted.

SYN and pad characters (leading and trailing) are provided by the attachment and are not stored in main storage.

Receive Synchronization

Character phase synchronization is established when two consecutive SYN characters followed by any non-SYN character are received and decoded. Character phase is maintained because the transmit station periodically inserts a synchronization pattern into the data stream.

The attachment deletes the SYN and pad characters and they are not put into main storage.

Time-Outs

There are three types of time-outs possible with BSC operations:

- Data set ready (DSR)
- Receive
- Program

Data Set Ready Time-Out

When performing an enable terminal operation, bit 12 of DCB word 0 can be used to cause the attachment to wait a predetermined time (13 seconds for single-line and 13 for multiline) for the modem to return the DSR. If DSR is not returned within this time period of DTR being activated, the attachment ends the operation and presents an exception interrupt request.

Receive Time-Out

The receive time-out is usually three seconds and causes the attachment to present an exception interrupt (CC2) under the following conditions:

- Character phase is not established within three seconds after the attachment accepts a receive data operation. This is under program control and is effective only if bit 12 is set to 1 in word 0 of the current DCB.

- A continuous synchronization pattern, or transparent synchronous idle (in transparent mode) is received for three seconds while in character phase.

- While receiving data, no synchronization pattern or transparent synchronization idle is received within three seconds.

Program Time-Out

A two-second time-out is available for use by the program. It is initiated by any Start command with bit 12 set to 1 in word 0 of the associated DCB. After two seconds, the attachment presents a device-end interrupt request (CC3).

Turnaround Considerations

When operating with modem eliminators, approximately 10 milliseconds (plus any associated program delays) should be allowed from the end of a write operation to the start of a read operation.

Commands

The Operate I/O instruction points to the immediate DCB (IDCB), which contains one of the following commands:

- Prepare
- Device Reset
- Halt I/O
- Read ID
- Start Control
- Start Diagnostic 1
- Start Diagnostic 2
- Start
- Start Cycle-Steal Status

The programmer should ensure that the program always tests the operate I/O condition codes following an Operate I/O instruction.

The programmer should also exercise care in modifying the DCB words before an interrupt request signifying the end of an operation. The attachment may not have fetched all of the DCB (due to the relatively slow speed of the attachment in relation to Series/1 processor instruction speeds).

Prepare

The Prepare command is used to control the interrupt parameters of the addressed device. The immediate data field of the IDCB contains the level and I-bit information. The single-line attachment is always able to accept and execute a Prepare command, even if it is busy or has an interrupt request pending from a previous command. On a multiple-line attachment, the device returns a condition code of 1 to this command if it has an interrupt request pending.

The IDCB for the Prepare command has the following format:

IDCB (immediate device control block)

Command field	Device address field
0 1 1 0 0 0 0 0	X X X X X X X X
0　　　　　　　7	8　　　　　　　15

　　　　　60　　　　　　　00—FF for multiple-line
　　　　　　　　　　　　　　　　attachments
　　　　　　　　　　　　　00—7F for single-line
　　　　　　　　　　　　　　　　attachments

Immediate data field		
0's	Level	I
16	26 27　　30	31
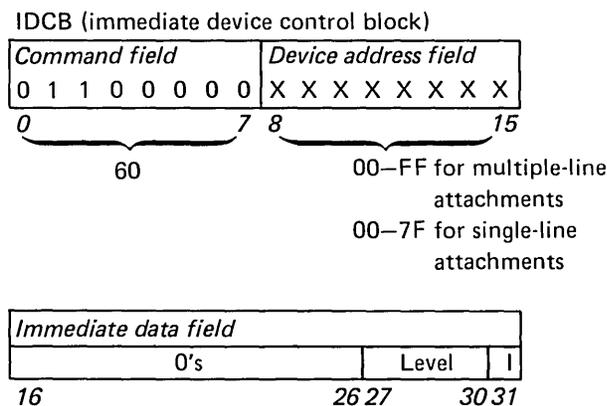
Level: This 4-bit field specifies the priority interrupt level assigned to the device.

Example

Bits 27–30	Level
0000	0
0001	1
0010	2
0011	3

A Prepare command issued to any device on a multiple-line attachment gives all of the devices in the attachment the same priority interrupt level. The I-bit information, however, applies only to the device addressed.

I-Bit: This bit determines whether the device is allowed to present interrupt requests. An I-bit value of 1 means that the device can request an interrupt; a value of 0 means that the device cannot interrupt.

The prepared attachment stores the level data and presents it to the processor each time an enabled device presents an interrupt request. This data is reset by a power-on reset. The prepare information can be changed by the successful execution of another Prepare command.

The Prepare command can allow an interrupt request to occur if the attachment is not prepared and has an interrupt request pending upon receipt of a Prepare with the I-bit set to 1.

The Prepare command always causes an attachment to respond with satisfactory (Operate I/O CC7) or device busy (on multiple-line controller only; CC1).

Device Reset

The Device Reset command resets the addressed device and clears any pending interrupt requests (except controller end). The Prepare information and the residual address do not change. Also, this command does not reset the DTR line to the modem or clear a controller end interrupt request.

IDCB (immediate device control block)

```
| Command field   | Device address field |
| 0 1 1 0 1 1 1 1 | X X X X X X X X |
  0             7   8            15
       6F                XX
```

```
| Immediate data field                    |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |
  16                             31
                   00
```
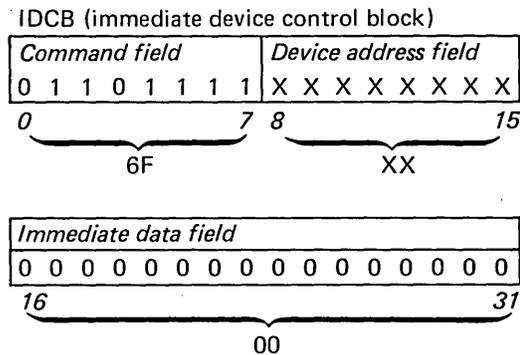
A Device Reset command issued to the attachment causes the attachment to become busy while the reset functions are carried out. The differences between the single-line attachment and the multiple-line attachment are:

• The length of time the attachment is busy performing the reset function

• The method used to report the conclusion to the program

For example, if a Start command follows a Device Reset too closely, a busy after reset (CC2) is reported on a single-line attachment. The program must reissue the command until a satisfactory (CC7) is reported.

On a multiple-line attachment, a controller busy (CC6) is reported when Start follows Device Reset too closely. When the reset is completed, the base address of the multiple-line controller (line 0) presents a controller end interrupt (CC0).

Note: Under certain conditions, it is possible that more than one controller end interrupt request is presented. If a busy condition is not found upon examining the controller busy queue, disregard the interrupt request.

Halt I/O

The Halt I/O command stops all I/O activity on the I/O channel. Any pending interrupt requests, including controller end (CC0), are cleared; the I-bits and priority level do not change. This instruction performs the same function as a system reset.

IDCB (immediate device control block)

```
| Command field   | Device address field |
| 1 1 1 1 0 0 0 0 | X X X X X X X X |
  0             7   8            15
       F0                XX
```
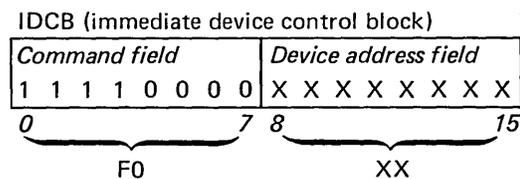
Read ID

The Read ID command puts the attachment's identification (ID) word into the immediate data field of the IDCB. The ID word contains physical information about the attachment that can be used to tabulate the system's configuration. The Read ID command is generally used in diagnostic programming.

IDCB (immediate device control block)

Command field	Device address field
0 0 1 0 0 0 0 0	X X X X X X X X
0 7	8 15
20	XX

Immediate data field
ID word
16   31
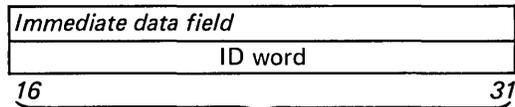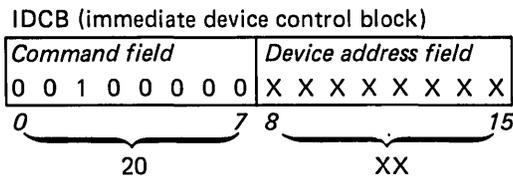
Single-line BSC	1006
Two-line BSC	2106
Four-line BSC	2206
Six-line BSC	2306
Eight-line BSC	2006

Note: If the control-feature card has jumpers installed for addresses not present, the controller responds to commands as if the hardware is present. Consequently, the ID of the controller should match the number of attachment lines present to prevent errors. For example, an ID of 2006 defines a multiple-line controller with two 4-line attachments (all eight lines in use). If there is one 4-line attachment present, the ID is 2206 (or 2106 if only two of the four lines are in use).

Start Control

The Start Control command is reserved for use by IBM engineering.

IDCB (immediate device control block)

Command field	Device address field
0 1 1 1 1 1 0 0	X X X X X X X X
0 7	8 15
7C	XX

Immediate data field
DCB address
16   31
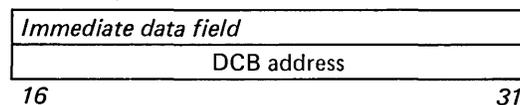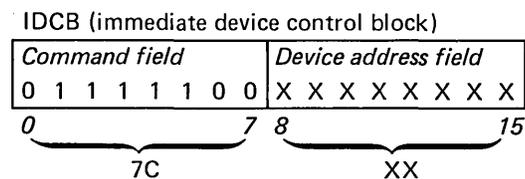
Issuing this command to a multiple-line attachment can cause the attachment to become inoperable. If this happens, the attachment can only be restored to operation by switching power off and then on again.

The format of the IDCB for this command is:

IDCB (immediate device control block)

Command field	Device address field
0 1 1 1 1 1 0 1	X X X X X X X X
0 7	8 15

$\underbrace{\qquad}_{7D}$ $\underbrace{\qquad}_{XX}$
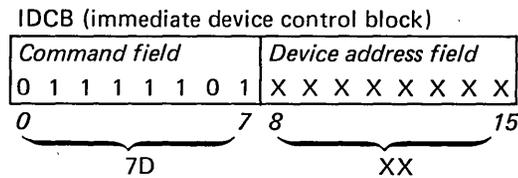
The format of the DCB for a Start Diagnostic 1 command follows:

Immediate data field
DCB address
16   31

$\underbrace{\qquad\qquad}_{XXXX}$
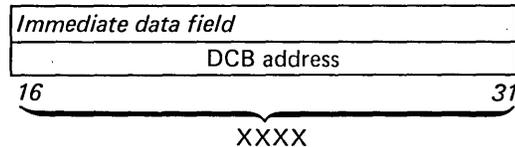
In the DCB control word, bit 2 must be set to 1 bits 5 through 7 can be set to either 0 or 1, and all other bits must be set to 0. The byte count must be 0008 (for single-line) or 000E (for multiple-line), and the data address must be even. If any of these conditions are not met. the attachment presents an exception interrupt request and reports a DCB specification check in the interrupt status byte.

This command causes the following two tests to occur in the attachment:
- A checksum test
- A register test

In the first test, the attachment calculates a checksum for each of the read-only storage modules in the attachment. Single-line attachments have two modules; multiple-line attachments have three. The read-only storage modules have a check sum built into them when they are made. The attachment transfers these four check sums to storage, beginning at the address specified in DCB word 7.

Data word 0 = Built in check sum - read-only storage 1
Data word 1 = Calculated check sum (inverted) - read-only storage 1
Data word 2 = Built in check sum - read-only storage 2
Data word 3 = Calculated check sum (inverted) - read-only storage 2
Data word 4 = Built in check sum - read-only storage 3 (see Note)
Data word 5 = Calculated check sum (inverted) - read-only storage 3 (see Note)
Data word 6 = AA55 (results of buffer test in addressed device)

Note: Reported by multiple-line attachments only.

The second test checks all registers in the attachment. If the test is successful, the attachment presents a device-end interrupt request. If an error is detected, the attachment halts and does not present a device-end interrupt request or an exception interrupt request.

Start Diagnostic 2

The format of the IDCB for the Start Diagnostic 2 command follows:
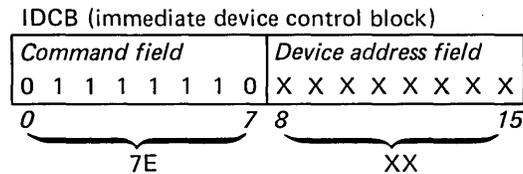
IDCB (immediate device control block)

Command field	Device address field
0 1 1 1 1 1 1 0	X X X X X X X X

0   7   8   15

       7E   XX

The format of the DCB for a Start Diagnostic 2 command follows:

Immediate data field
DCB address

16   31

            XXXX
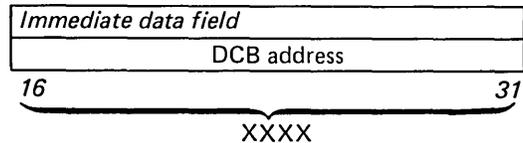
In the DCB control word, bit 2 must be set to 1, bits 5–7 can be set to either 0 or 1 and all other bits must be set to 0. The byte count must be 0002 (for both single-line and multiple-line attachments), and the data address must be even. If any of these conditions are not met, the attachment presents an exception interrupt request and reports DCB specification check in the interrupt status byte.

The attachment activates DTR and request-to-send (RTS) and checks for DSR and clear-to-send (CTS) to be returned through the modem cable and wrap connector. The attachment then checks the serializer/deserializer (SERDES) by wrapping a data character through the cable and wrap connector. The results of this test are then placed into the high-order byte of the storage data register. The bits in this byte are:

Bit	Meaning
0	Data terminal ready
1	Data set ready
2	Request-to-send
3	Clear-to-send
4	Clocks found (see Note)
5	Buffer service latch failed to set
6	Transmit mode latch (should equal 1)
7	Data wrap failed

Note: Bit 4 is set to 1 if both transmit and receive clocks are activated due to internal clocking being wired on. The correct results of this test are F2XX or FAXX, depending on whether internal clocking is being used.

The attachment places hex FF into the low-order byte of the storage data register and then attempts to transfer only the high-order byte to storage. Only the high-order byte of the word in storage addressed by DCB word 7 should be changed. The program should load a value other than hex FF into the low-order byte of storage so that it can determine if the byte mode transfer worked. If the byte mode generated an error, the low-order byte in storage contains hex FF.

The Start command initiates a cycle-steal operation for the addressed device. The format of the IDCB for the Start command is:

IDCB (immediate device control block)

Command field	Device address field
0 1 1 1 0 0 0 0	X X X X X X X X

0 ───────────── 7 8 ───────────── 15

_____70_____   _____XX_____

The format of the DCB for the Start command follows:

Immediate data field
DCB address

16 ──────────────────────────── 31

XXXX

DCB Word 0 - Control

Bit 0 - Chaining Flag: If this bit is set to 1, the attachment fetches the next DCB in the chain at the end of the current DCB operation.

Note: Chaining should not be used to receive continuous blocks of data in the high-speed attachment (greater than 9,600 bps), or the multiple-line attachment. Overrun errors may occur if receive operations are chained in these attachments.

Bit 1: Not used, set to 0.

Bit 2 - Input Flag: If bit 2 is set to 1, data is transferred from the attachment to the processor; if bit 2 is set to 0, data is transferred from the processor to the attachment.

On a Start command, this bit set to 1 specifies a receive operation.

The receive operation allows the attachment to start transferring data to main storage after character synchronization is established.

The attachment presents a normal device-end interrupt request or begins a DCB command chaining operation when a COD character is received and the byte count is reduced to 0.

The attachment presents an exception interrupt request and interrupt status byte bit 1 is set to 1 if DSR equals 0 when the operation begins.

Bit 12 of DCB word 0 can be used with this operation to limit the time the attachment allows for establishing character synchronization to 3 seconds. Failure to establish character synchronization within this time results in an exception interrupt request with interrupt status byte bit 0 set to 1.

Bits 3-4: Not used, set to 0.

Bits 5-7 - Cycle-Steal Address Key: A 3-bit key presented to the processor by the attachment during cycle-steal data transfers. It is processor to determine if the attachment is authorized to access certain blocks of main storage.

Bit 8 - Half-Rate: The attachment uses this bit only during the enable terminal operation. If bit 8 is set to 1, the modem (if it is equipped to recognize half-rate) runs at one-half of its normal bit rate. If internal clocking is being used, this bit selects the 600-bps rate. If the state of the rate-select line is to change, the attachment automatically waits 13 seconds before checking for DSR. This allows the modem enough time to equalize.

Note: If this bit is set to 1 and the attachment generates an answer tone, it resets the bit rate to its previous speed. Another enable terminal operation is required to set half-rate again.

Bit 9 - ASCII Mode: If this bit is set to 1, the attachment uses ASCII; if the bit is set to 0, the attachment uses EBCDIC.

Bit 10 - Enable Terminal: This bit is used to activate DTR to the modem. A device-end interrupt request occurs 50 milliseconds after DSR is returned by the modem. If DSR is already active, the request occurs immediately.

Bit 12 can be used in conjunction with this operation to limit the time that the attachment waits for DSR to become active. If bit 12 is set to 1, failure to get DSR within 13 seconds results in DTR being reset and an exception interrupt request with interrupt status byte bit 0 set to 1.

On a medium-speed, single-line attachment wired to IPL the Series/1 processor in a switched network, a ring indication from the modem also sets DTR to 1. For manual call or manual answer sequence, bit 10 must be used to set DTR to 1 before entering data mode.

On a leased line, DTR is normally set to 1.

Bit 11 - Disable Terminal: Causes the attachment to deactivate DTR in order to disconnect the modem from a switched network. The attachment presents a device-end interrupt request or begins a chaining operation 2 seconds after DSR goes off. If DSR is not deactivated within 3 seconds, the attachment presents an exception interrupt request with interrupt status byte bit 0 set to 1.

Bit 12 - Start Timer: Can be used with an enable terminal operation or with a receive operation to provide a 3-second time-out. When used alone, bit 12 causes the attachment to start timing a 2-second period, after which the attachment presents a device-end interrupt request.

Bit 13 - Transmit Operation: Starts a 3-second timer and turns on RTS. When the modem returns CTS, the attachment establishes synchronization (described under "Synchronization and Timing" earlier in this chapter). The attachment then starts fetching data from main storage and transmitting the data.

The attachment presents a normal device-end interrupt request or begins a DCB command chaining operation when a line turnaround character (COD) is transmitted and the byte count goes to 0.

The attachment presents an exception interrupt request and interrupt status byte bit 0 is set to 1 if DSR is set to 0 when the operation begins.

Failure to receive CTS from the modem within the 3-second time-out period or CTS being active for 3 seconds without RTS being active results in an exception interrupt request with bit 0 set to 1 in the interrupt status byte.

The attachment resets transmit mode and RTS after transmitting the pad character following a COD character. If block checking is used, the attachment resets transmit mode and RTS after transmitting the pad character following the BCC.

Note: RTS can be permanently wired on when desired. CTS must not be permanently returned by the modem unless RTS is wired on.

Bit 14 – Exit Transparent: Because the BSC attachment does not recognize control characters when transmitting in transparent text mode, there must be a method of transmitting control sequences so that they can be recognized as such. This is accomplished by the exit transparent operation.

The exit transparent operation requires its own DCB and a byte count of 2. Unexpected results can occur if the byte count is greater than 2.

This operation should be used only to transmit the control sequences shown below following a block of transparent text.

- DLE-ETX
- DLE-ETB
- DLE-ITB
- DLE-ENQ

Bit 15: Not used, set to 0.

DCB Words 1-4

Not used.

DCB Word 5 – Chaining Address

Contains the storage address of the next DCB and is used when chaining is indicated. The chaining address must be even. If it is odd, the attachment sets interrupt status byte bit 3 to 1 and ends the operation.

DCB Word 6 – Byte Count

Contains the number of bytes to be transferred to or from storage.

DCB Word 7 – Data Address

The address in processor storage where data transfer is to start.

Start Cycle-Steal Status

The Start Cycle-Steal Status causes the device to initiate a cycle-steal operation for the purpose of collecting status information about the previous cycle-steal operation. The format of the IDCB for this command follows:

IDCB (immediate device control block)

Command field	Device address field
0 1 1 1 1 1 1 1	X X X X X X X X
0 7	8 15

7F   XX

The format of the DCB for a Start Cycle-Steal Status command follows:

Immediate data field
DCB address
16   31

XXXX

The byte count in the DCB (word 6) must be equal to 6 and the data address (word 7) must be on a word boundary (bit 15 set to 0) or an exception interrupt request (CC2) occurs with DCB specification check bit (bit 3) set to 1 in the interrupt status byte.

Three words of status information are available by using the Start Cycle-Steal Status command.

The format of the DCB for this command is the same as for a normal cycle-steal data transfer. The chaining bit is not checked by the attachment, but it should be set to 0. The byte count must be 6. Six bytes of information are transferred to main storage starting at the data address contained in DCB word 7.

Status Word 0

Word 0 contains the main storage address of the last attempted cycle-steal data transfer. This residual address may be either a data or a DCB address. When reporting a DCB address, the attachment reports the address of the low-order byte of the last DCB word that the attachment attempted to fetch.

Status Word 1

Bit 0 - Overrun: During a receive operation, this condition occurs if the attachment is unable to transfer the contents of the storage data register to main storage before it is time to reload the register. During a transmit operation, an overrun occurs if the attachment is unable to reload the storage data register in time to keep a steady stream of data going out on the line.

Bit 1 - Time-Out: Set to 1 if:
* DSR is not received from the modem within 3 seconds after an enable terminal operation begins (if bit 12 of DCB word 0 is set to 1).
* Character phase is not established within 3 seconds of acceptance of a receive operation (if bit 12 of DCB word 0 set to 1).
* A continuous synchronization pattern is received for 3 seconds.
* While receiving data, no synchronization pattern is received for a period of 3 seconds.

Bit 2 - Modem Interface Error: Conditions that cause this error are:
* DTR or DSR set to 0 at the beginning of a transmit or a receive operation.
* CTS set to 1 for more than 1 second while RTS set to 0 at the beginning of a transmit operation.
* DTR or DSR is lost during a transmit or a receive operation.
* RTS or CTS is lost during a transmit operation.
* CTS is not returned by the modem within 3 seconds after the attachment activates RTS.

Bit 3 - Block Check Error: The BCC received over the data link does not compare with the BCC accumulated in the attachment. In ASCII mode, an LRC or VRC error is indicated by this bit.

Note: This error may also occur during heavy channel activity.

Bit 4 - Multipoint Transmit Error: Indicates that the attachment is a tributary on a multipoint network and a transmit operation was attempted before the controlling station selected this station.

Bit 5 - Answer-Tone Jumper Installed: Indicates that the attachment is wired to provide an answer tone when it senses that the ring indicator line from the modem is active.

Bit 6 - Multipoint Tributary Jumper Installed: Indicates that the attachment is a tributary station in a multipoint network.

Bit 7 - Internal Clock Jumper Installed: Indicates that the internal clock jumper is installed in the attachment. The attachment provides clocking for 1,200 bps (600 bps if half-rate has been specified in the control word of the DCB).

Bits 8-15 - Multipoint Address: Indicates that this is the multipoint address for which the attachment is wired. Bit 8 equals multipoint address bit 0; bit 15 equals multipoint address bit 7.

Note: On single-line attachments, bit 8 (multipoint address bit 0) allows the attachment to IPL the processor when this bit is set to 1, regardless of whether or not the attachment is a multipoint tributary. Bit 0 must not be set to 1 when using ASCII.

Status Word 2

Word 2 contains status information regarding certain key lines of the device and indicates that the following modem lines or conditions are active.

Bit 0 - Data Terminal Ready: An outbound signal from the attachment to the modem indicating that the attachment is ready to communicate.

Bit 1 - Data Set Ready: An inbound signal to the attachment from the modem indicating that power is on and the modem is ready for line operations.

Bit 2 - Request-to-Send: An outbound signal from the attachment to the modem requesting that the modem prepare for data transmission.

Bit 3 - Clear-to-Send: An inbound signal to the attachment from the modem indicating that the link is ready to transmit data.

Bit 4 - Ring Indicator: An inbound signal to the attachment indicating that the modem detects a ring condition on the line; this is reported to the program as an attention interrupt request.

Bit 5 - Half-Rate Selected: An outbound signal to the modem indicating that it should operate at half-normal speed (modem must be equipped with this option); the signal is also called data signal rate selector.

Bit 6 - Transmit Mode Latch: Indicates that the attachment is transmitting data.

Bit 7: Not used, set to 0.

Bits 8-15 - Indicator Panel Switch Setting: Indicates the current setting of the communications indicator panel DISPLAY/FUNCTION SELECT switches (if installed); bits set to 0 if communications panel is not installed.

Condition Codes and Status Information

Operate I/O Instruction Condition Codes

The BSC single-line and 8-line control feature may present a variety of operate I/O condition codes; these are shown below for each type of Operate I/O command with a recommended action.

BSC operate I/O condition codes

CC value	Even	Carry	Overflow	Meaning
0	0	0	0	Not attached
1	0	0	1	Busy
2	0	1	0	Busy after reset (Note 1)
3	0	1	1	Command reject
4	1	0	0	Intervention required (Note 2)
5	1	0	1	Interface data check
6	1	1	0	Controller busy (Note 3)
7	1	1	1	Satisfactory

Notes:

1. Not reported by the multiple-line attachment.

2. Not reported by any communications attachment.

3. Not reported by any single-line communications attachment. Reported on multiple-line attachments when the controller is busy servicing a previous Operate I/O instruction; a subsequent controller-end interrupt occurs (interrupt condition code 0).

Interrupt Condition Codes

Interrupt requests can occur for the BSC attachment only following the acceptance of these commands:

- Prepare (this command is not normally an interrupting command. The only time an interrupt request can occur following this command is when the device is unprepared and an interrupt request is pending).
- Start Control (multiple-line attachment only)
- Start Diagnostic 1
- Start Diagnostic 2
- Start
- Start Cycle-Steal Status

CC value	Even	Carry	Overflow	Meaning
0	0	0	0	Controller end (Note 1)
1	0	0	1	PCI (Note 2)
2	0	1	0	Exception
3	0	1	1	Device end
4	1	0	0	Attention
5	1	0	1	Attention and PCI (Note 2)
6	1	1	0	Attention and exception
7	1	1	1	Attention and device end

Notes:

1. Reported only by multiple-line attachment. The controller presents the device address of line 0.

2. Not reported by BSC attachments.

Various combinations of interrupt condition codes and interrupt status byte values with recommended actions follow:

Interrupt status byte

Bit	Name
0	Device-dependent status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage check
5	Invalid storage address
6	Protection check
7	Interface data check

Status

Interrupt Status Byte

When the attachment presents an interrupt request to the processor, the interrupt status byte is used to record status that cannot be indicated to the program by condition codes. The interrupt status byte is meaningful only when interrupt condition code 2 or 6 is reported. The processor detects the interrupt status byte in bits 0 through 7 of the interrupt ID word.

Bit 0 - Device-Dependent Status Available: If this bit is set to 1, additional status is available by using the Start Cycle-Steal Status command (a discussion of this status follows in this chapter). This bit may be set to 1 in conjunction with bit 2 (incorrect length record).

Bit 1 - Delayed Command Reject: Set to 1 under the following conditions:

- The command field of the IDCB contains an invalid function or modifier bit combination.
- The IDCB contains an odd DCB address.
- The command field of the IDCB specified a Write command: (010X XXXX).

Bit 2 - Incorrect Length Record: This error can occur during both transmit and receive operations. It is caused by either of the following conditions:

- The byte count has been decremented to 0, the attachment has not detected a COD character, and the chaining flag is off.
- The attachment has detected a COD character and the byte count has not been decremented to 0.

In this case, interrupt status byte bit 0 also is set 1. A Start Cycle-Steal Status command can be used to determine the location of the COD in storage (residual address).

Bit 3 - DCB Specification Check: Any of the following conditions cause this error:

- Word 5 of the DCB (chain address) contains an odd address.
- Word 6 of the DCB (byte count) contains a count other than 6 for a Start Cycle-Steal Status command.
- Word 7 of the DCB (data address) contains an odd address for a Start Cycle-Steal Status command.
- A byte count of 0 is specified in the DCB for either a transmit or receive operation.
- Bit 2 of the DCB control word is set to 0 for a Start Cycle-Steal Status command.
- Bit 3 of the DCB control word is set to 1.

Bit 4 - Storage Data Check: Set to 1 during cycle-steal output operations only. It indicates that the main storage location accessed during the current output cycle contains incorrect parity. The attachment ends the operation with an exception-interrupt request.

Bit 5 - Invalid Storage Address: Set to 1 if the address presented by the attachment for data or DCB access exceeds the storage size of the system. The attachment ends the operation with an exception- interrupt request.

Bit 6 - Protect Check: Set to 1 if the attachment attempts to access a storage location without the correct cycle-steal address key.

Bit 7 - Interface Data Check: Equals 1 if a parity error has detected an interface cycle-steal data transfer. The condition can be detected by the channel or the attachment. In either case, the attachment ends the operation with an exception-interrupt request.

Status After Reset

There are several methods of resetting some or all of the circuits in the attachment. They are:

Reset	Action
Power-on reset	All attachment components are reset to the off condition.
System reset/device reset	All attachment components (except DTR latches and the cycle-steal residual address) are reset to the off condition. The controller end interrupt request is not affected by a device reset.

Note: For a system reset, Device Reset command, or Halt I/O command, the information displayed by indicator panel switch settings 0-C is not reset.

Multiple-Line Attachment Operation

The BSC multiple-line attachment controller is designed to service one or two binary synchronous communication 4-line adapter features. The BSC multiple-line attachment contains hardware and a microprocessor to service the 4-line adapter. The basic difference between the multiple-line attachment and the single-line attachment (other than speed limitations) is that the multiple-line attachment presents a controller busy operate I/O condition code to the program, followed by a controller-end interrupt request when its hardware is no longer busy.

When multiple controller busy operate I/O condition codes are presented, there can be one controller-end interrupt request. The programmer should queue the controller busy Operate I/O condition codes and clear (post) the controller-end interrupt condition code to all the controller busy codes received.

Jumper Options

The following options can be selected by installing jumpers on the feature cards.

Single-Line Control Feature/Medium Speed

Internal Clocking: With this jumper installed the attachment provides clocking, selected by programming, at 1,200 bps or 600 bps.

Answer Tone: With this jumper installed, the attachment provides a 3-second answer tone after the modem activates DSR in response to the attachment activating DTR. This jumper should not be installed if the modem provides an answer tone.

Request-to-Send: If this jumper is installed, the attachment maintains RTS in an active condition. This eliminates modem turnaround when using a duplex modem. This option should always be selected when using a modem that always keeps CTS active.

Data Terminal Ready: If this jumper is installed, the attachment maintains DTR in an active condition. This option must not be selected for switched-line operation.

No Ring Indication: This jumper must be installed if the modem does not provide a ring indication.

Multipoint Tributary: This jumper is installed if the attachment is to be used as a multipoint tributary. It causes the attachment to look for its multipoint address on the receive-data line after receiving an initial character synchronization sequence.

Multipoint Address: These jumpers establish the multipoint address to which the attachment is to respond. If bit 0 is set to 1, the attachment is allowed to respond to a host-initiated IPL sequence, regardless or whether or not the multipoint tributary jumper is installed. Bit 0 must **not** be set to 1 when using ASCII.

For switched-line operation, bit 7 must be set to 1, and the multipoint tributary jumper must not be installed.

Single-Line Control Feature/High Speed

The high-speed attachment provides the following options which perform functions identical to those described for the medium-speed single-line attachment:

- Request to send
- Data terminal ready
- Multipoint tributary
- Multipoint address

In addition to the above options, the attachment has jumpers to select either an interface compatible with a Western Electric 303 Data Set (or equivalent) or an interface compatible with CCITT recommendation V.35.

4-Line Adapter Feature

The jumpers on this feature are the same as the jumpers on the medium-speed, single-line attachment except that multipoint address bit 0 has nothing to do with IPL because multiple-line attachments cannot IPL. There are four complete sets of jumpers on each card, one set for each line.

Communications Indicator Panel

This optional panel is a valuable aid to program debugging and machine trouble-shooting.
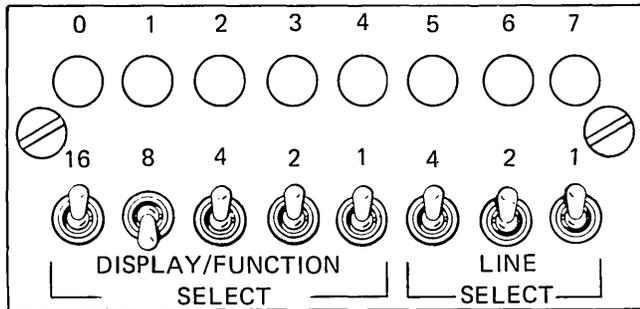
LINE SELECT Switches

The three LINE-SELECT switches are used only with multiple-line attachments to select a particular line. A line is selected by setting the last three bits of its device address, in binary form, into the LINE-SELECT switches. The LINE-SELECT switches are ignored when the indicator panel is used with a single-line attachment.

DISPLAY/FUNCTION SELECT Switches

The DISPLAY/FUNCTION SELECT switches determine what information is displayed on the panel. Following are lists of switch settings and the information that is displayed on the panel.

DISPLAY/ FUNCTION SELECT switch setting	Lamps	Information
00000	0–7	High-order byte of DCB word 0 (control word)
00001	0–7	Low-order byte of DCB word 0 (control word)
00010	0–7	High-order byte of DCB word 5 (chain address)
00011	0–7	Low-order byte of DCB word 5 (chain address)
00100	0–7	High-order byte of DCB word 6 (byte count)
00101	0–7	Low-order byte of DCB word 6 (byte count)
00110	0–7	High-order byte of DCB word 7 (data address)
00111	0–7	Low-order byte of DCB word 7 (data address)
01000	0–7	High-order byte of the storage data register
01001	0–7	Low-order byte of the storage data register
01010	5	Interrupt condition code bit 4
	6	Interrupt condition code bit 2
	7	Interrupt condition code bit 1
01011	0–7	ISB
01100	0–7	High-order byte of cycle-steal status word 1
01101	0–7	High-order byte of the CRC
01110	0–7	Low-order byte of the CRC (or LRC)
01111	0	DTR
	1	DSR
	2	RTS
	3	CTS
	4	Ring indicator
	5	Half-rate select
	6	Transmit mode
10000	0	DTR
	1	DSR
	2	RTS
	3	CTS
	4	Transmit data (on = space)
	5	Receive data (on = space)
	6	Transmit mode
	7	Receive mode

DISPLAY/ FUNCTION SELECT switch setting	Lamps	Information
10001	5	Answer-tone jumper installed
	6	Multipoint tributary jumper installed
	7	Internal clocking jumper installed
10100	0–7	Multipoint address
10110	0	COD
	1	BCC
	2	Text Mode
	3	Transparent mode
	4	DLE 1
	5	Character phase
	6	SYN 2
	7	SYN 1
10111	0	Selected mode
	1	Control mode
	2	VRC error
	3	BCC error
	4	ASCII mode
11000	0	Second DC1
	1	First DC1 IPL sequence
	2	Address 2 (MP address received)
	3	Address 1 (MP address received)
11010	5	ITB sent or received
	6	EOT/NAK sent or received
11011	3	EOT sent or received
11100	0–7	Lamp test; all lamps should be on
11111	0–7	Same as switch setting 10000; resets DTR.

Note: Switch settings and lamp indications other than those shown require detailed knowledge of the microcode to understand.

DISPLAY/ FUNCTION SELECT switch setting	Lamps	Information
00000	0–7	High-order byte of DCB word 0 (control word)
00001	0–7	Low-order byte of DCB word 0 (control word)
00010	0–7	High-order byte of DCB word 5 (chain address)
00011	0–7	Low-order byte of DCB word 5 (chain address)
00100	0–7	High-order byte of DCB word 6 (byte count)
00101	0–7	Low-order byte of DCB word 6 (byte count)
00110	0–7	High-order byte of DCB word 7 (data address)
00111	0–7	Low-order byte of DCB word 7 (data address)
01000	0–7)	High-order byte of the storage data register
01001	0–7)	Low-order byte of the storage data register
01010	5	Interrupt condition code bit 4
	6	Interrupt condition code bit 2
	7	Interrupt condition code bit 1
01011	0–7	ISB
01100	0–7	High-order byte of cycle-steal status word 1
01101	0–7	High-order byte of the CRC
01110	0–7	Low-order byte of the CRC (or LRC)
01111	0	DTR
	1	DSR
	2	RTS
	3	CTS
	4	Ring indicator
	5	Half-rate select
	6	Transmit mode
10000	0	DTR
	1	DSR
	2	RTS
	3	CTS
	4	Transmit data
	5	Receive data
	6	Transmit mode
	7	Receive mode
10001	4	Interrupt pending
	5	Answer tone jumper installed
	6	Multipoint tributary jumper installed
	7	Internal clocking jumper installed
10100	0–7	Multipoint address
10101	0	Enable timer bit
	1–7	Timer value in 50-milliseccond increments

DISPLAY/ FUNCTION SELECT switch setting	*Lamps*	*Information*
10110	0	COD sent or received
	1	BCC sent or received
	2	Text Mode
	3	Transparent mode
	4	DLE sent or received
	5	Character phase
10111	0	Selected mode
	1	Control mode
	2	VRC error
	3	BCC error
11000	2	Address 2 (MP address received)
	3	Address 1 (MP address received)
11001	1	ITB sent or received
	2	EOT/NAK sent or received
	7	EOT sent or received
11100	0–7	Lamp test; all lamps should be on
11101	0–7	First character after character phase in receive
11110	0–7	Contains last COD character sent or received
11111		Resets DTR if it is not jumpered on

Note: Switch settings and lamp indications other than those shown require detailed knowledge of the microcode to understand.

Error Recovery

Error recovery for the Binary Synchronous Communications is as follows:

1. Inspect the Operate I/O condition code and use the following chart:

Command	Operate I/O CC	Recommended action
Read ID	0	End (device not attached).
	1,2,4,6	End (hardware error).
	3	Examine the IDCB function modifier; end if IDCB is correct.
	5	Retry three times; end if problem persists.
	7	Satisfactory.
Prepare	0	End (device not attached).
	1	End if single-line; if multiple-line, examine bit 15; if bit 15 is set to 1, end; if bit 15 is set to 0, correct program.
	2,4,6	End.
	3	Examine the IDCB function modifier; end if IDCB is correct.
	5	Retry three times; end if the problem persists.
	7	Satisfactory.
Halt I/O	0,1,2,3,4,5,6	End (equipment error).
	7	Satisfactory.
Device Reset	0	End (device not attached).
	1,2,4,6	End (equipment error).
	3	Examine IDCB function modifier; end if the IDCB is correct.
	5	Retry three times; end if the problem persists.
	7	Satisfactory.
Start, Start Cycle-Steal Status, Start Diagnostic 1 and 2 and Start Control (multiple-line only)	0	End (device not attached).
	1	Issue a Device Reset; retry; end if the problem persists.
	2	If present on muliple-line adapter, end. If single-line attachment, retry; end if problem persists.
	3	Examine the IDCB function modifiers; end if the IDCB is correct.
	4	End.
	5	Retry three times; end if the problem persists.
	6	If multiple-line adapter, retry after controller end interrupt. If single-line attachment, end.
	7	Satisfactory.

2. Inspect the interrupt condition code.

- If the interrupt condition code is 3, end.
- If the interrupt condition code is a 2 or a 6, use the following chart.

Interrupt status byte (hex)	Recommended action
A0	Normal ending operation to a receive DCB; if a COD was detected before reducing the byte count to 0, perform a Start Cycle-Steal Status command to obtain the location of the COD (residual address)
80	Issue a Start Cycle-Steal Status command, and examine bits for determination of further action
40	Examine IDCB for invalid function modifier or odd DCB address; correct error condition and retry
20	Occurs during a receive or transmit operation; indicates that the byte count reduced to 0 and no COD character was detected; increase the receive data buffer size and byte count and retry
10	Indicates that the DCB being executed had an odd chain address (word 5); a Start Cycle-Steal Status DCB had a byte count other than 6 or an odd address; a transmit or receive DCB had a byte count of 0; the I/O bit of the DCB control word is incorrect; a diagnostic type DCB had incorrect byte count or odd data address; a Start Control command to a multiple-line attachment did not have a byte count of hex 300 or had an odd data address; correct the error and retry
08	Storage data check; retry operation; if error persists, end
04	Invalid storage address; correct program and retry
02	Protect check; verify the protect key and retry;
01	Interface data check; retry once and end if the error persists

Appendix A. BSC Reference Summary

I/O Commands

Hex	Command	I/O instruction CCs reported
20	Read ID	0,1*,2*,5,7
60	Prepare	0,1**,5,7
6F	Device Reset	0,7
70	Start	0,1,2*,5,6**,7
7C	Start Control	0,1,2*,5,6**,7
7D	Start Diagnostic 1	0,1,2*,5,6**,7
7E	Start Diagnostic 2	0,1,2*,5,6**,7
7F	Start Cycle-Steal Status	0,1,2*,5,6**,7

*Not reported by the multiple-line attachments.

**Not reported by any single-line communications attachment.

Device Control Block (DCB)

Word		
0	Control word	
1	Not used	
2	Not used	
3	Not used	
4	Not used	
5	Chain address	
6	Byte count	
7	Data address	

0   15

Control Word

Bit	Meaning
0	Chaining flag
1	Not used - zero
2	Input flag
3	Not used - zero
4	Not used - zero
5-7	Cycle-steal address key
8	Half rate
9	ASCII mode
10	Enable terminal
11	Disable terminal
12	Start timer
13	Transmit operation
14	Exit transparent
15	Not used - zero

Cycle-Steal Status Words

Word 0

Bit	Meaning
0-15	Residual address

Word 1

Bit	Meaning
0	Overrun
1	Timeout
2	Modem interface error
3	Block check error
4	Multipoint transmit error
5	Answertone jumper installed
6	Multipoint tributary jumper installed
7	Internal clock jumper installed
8-15	Multipoint address

Word 2

Bit	Meaning
0	Data terminal ready
1	Data set ready
2	Request-to-send
3	Clear-to-send
4	Ring indicator
5	Half rate selected
6	Transmit mode latch
7	Not used - zero
8-15	Indicator panel switch setting

Interrupt Condition Codes Reported

CC0*, CC2, CC3, CC4, CC6, CC7

*Not reported by single-line attachments.

Interrupt Information Byte (IIB)

Condition Code	IIB Contents
0, 3, 4, 7	Always zero
2, 6	Determined by halt ISB (hex) value

Interrupt Status Byte (ISB)

Bit	ISB meaning
0	Device status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check*
7	Interface data check

*Zero for a device attached to a 4952 or 4953 processor.

Appendix B. Communications Operator's Self-Test Procedure

The communication adapters operator self-test program needs a minimum system configuration of:

- a Series/1 processor with 16K storage
- a diskette drive feature 4964 or 4962 model 2
- a programmer console feature 5650, and
- one communication adapter feature 2074, 2093/2094.

1. Remove power, disconnect the modem cable at the modem and connect the wrap connector at the modem end of the cable as follows:

Modem cable part number	Wrap connector part number
1632208	2704136
1632211	1633811
1632919	*

*Do not disconnect the modem cable but place the switch in the cable extension part number 2722052 in the test position.

2. Insert the basic diskette.

3. Press the load button on the programmer console.

4. If the system has only a programmer console go to step 10.

5. Wait for the input/output device (as configured in the diagnostic diskette) to print the following message:

   RDY

   ENTER

6. Begin the operator self-test program be entering B3CEF on the input/output device.

7. The output device will then print:

   ENTER DEVICE ADDRESS AND LOOP COUNT

   ENTER

8. Enter FDAXX (where DA=device address and XX=loop count in hexadecimal).

   Example:

   F1801 (DA=18, loop count=01).

9. Wait for one of the following messages to appear, then take the appropriate operator action:

Message:

DEVICE ADDRESS ERROR

REENTER DEVICE ADDRESS AND LOOP COUNT

ENTER

Operator action:

Verify that the device address is correct and call the service organization or return to step 8.

Message:

TEST WAS SUCCESSFUL

Operator action:

None, self-explanatory.

Message:

THE TEST FAILED, CALL THE SERVICE ORGANIZATION

Operator action:

Verify that the cable and wrap connector have the correct part numbers and call the service organization or return to step 8.

After the loop count has been exhausted, the program returns to step 7. At this time, you may run the test again or end the program by returning the system to the operating state. (Steps 10 through 16 of this procedure are for systems with only a programmer's console.)

Note: The running time for each feature per pass is as follows:

Feature	Time
2074	1 second
2093/2094	8 seconds

10. Wait for a hexadecimal 3800 in the lights of the programmer console.
11. Insert the SIO/communications diskette.
12. Press the data buffer button and enter 000B, then press the console interrupt button. Press the data buffer button again and enter 3CEF, then press the console interrupt button twice.

13. Wait for 3CE1 on the lights of the programmer console.

14. Press data buffer and enter 001F, then depress the console interrupt button.

15. Press the data buffer and enter DAXX (where DA=device address and XX=loop count). Press the console interrupt button twice.

16. Wait for one of the following values to appear in the lights of the programmer console.

Value in lights	Operator action
3CE2 (Device address error)	Verify the address is correct and call the service organization or go to step 1.
3CE3 (Test successful)	Self-explanatory
3CE4 (The test failed, call the service organization	Verify that the cable wrapped in the correct one and call the service organization or return to step 11.

17. Press the data buffer button, enter 0006, and press the console interrupt button twice. Wait for the lights to indicate 3CE1 and proceed to step 13 to run the test again, if desired, or return the system to the operating state.

Appendix C. BSC Adapter Initialization Programs

BSC Adapter Initialization Program
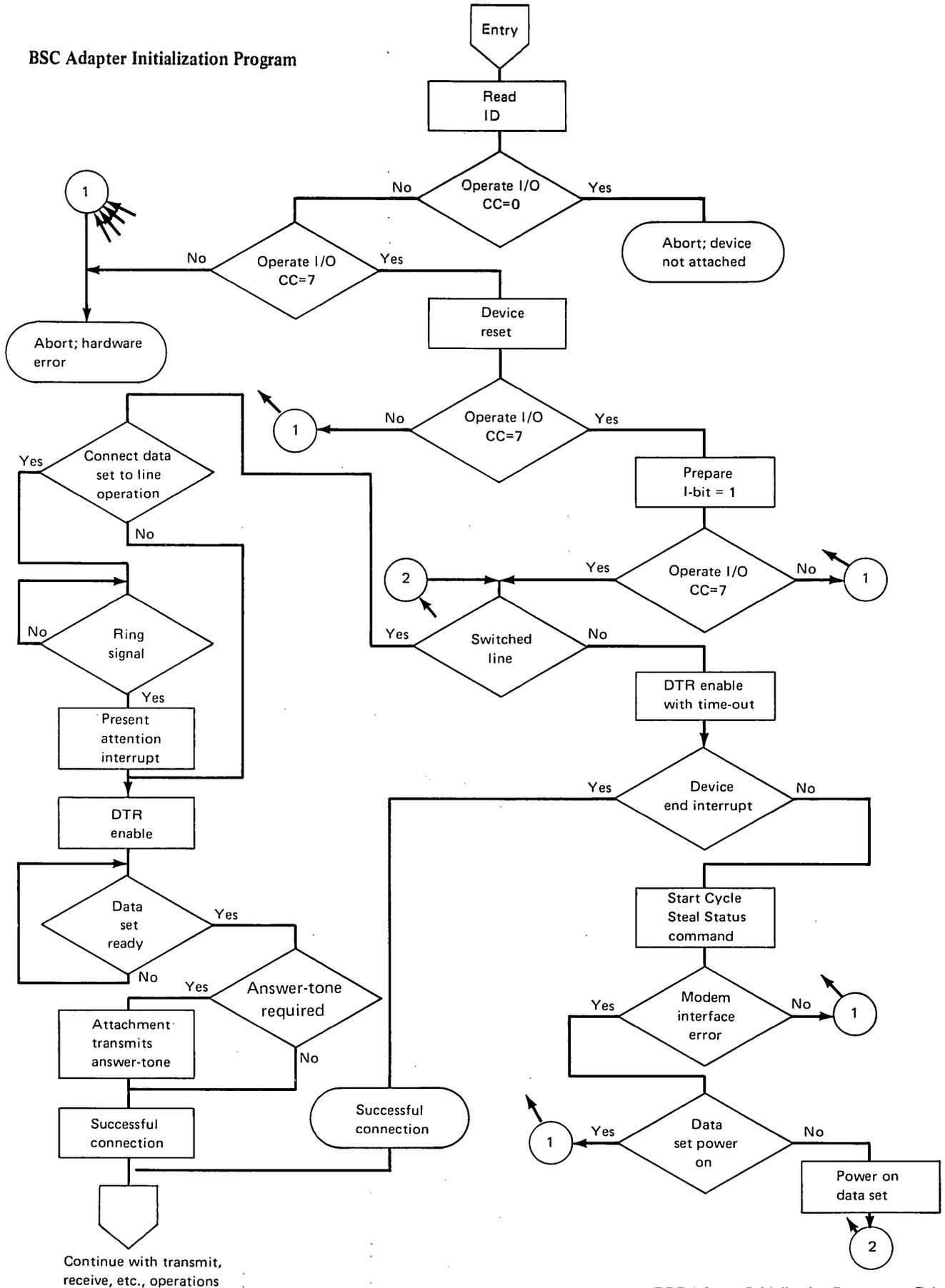
Continue with transmit,
receive, etc., operations

Appendix D. Transmission Codes

Decimal	Hex	Binary	EBCDIC	ASCII (see note)	Eight-bit data interchange	PTTC/EBCD	PTTC/correspondence
0	00	0000 0000	NUL	NUL	NUL		
1	01	0001	SOH	SOH	NUL	space	space
2	02	0010	STX	STX		1	1,]
3	03	0011	ETX	ETX	@		
4	04	0100	PF	EOT		2	2
5	05	0101	HT	ENQ	space		
6	06	0110	LC	ACK			
7	07	0111	DEL	BEL		3	3
8	08	1000		BS		4	5
9	09	1001	RLF	HT			
10	0A	1010	SMM	LF	P (even parity)		
11	0B	1011	VT	VT	P (odd parity)	5	7
12	0C	1100	FF	FF	0 (even parity)		
13	0D	1101	CR	CR	0 (odd parity)	6	6
14	0E	1110	SO	SO		7	8
15	0F	1111	SI	SI			
16	10	0001 0000	DLE	DLE		8	4
17	11	0001	DC1	DC1			
18	12	0010	DC2	DC2	H (even parity)		
19	13	0011	TM	DC3	H (odd parity)	9	0
20	14	0100	RES	DC4	((even parity)		
21	15	0101	NL	NAK	((odd parity)	0	z
22	16	0110	BS	SYN		Ⓓ (EOA)	Ⓓ (EOA),9
23	17	0111	IL	ETB			
24	18	1000	CAN	CAN			
25	19	1001	EM	EM			
26	1A	1010	CC	SUB			
27	1B	1011	CU1	ESC	X		
28	1C	1100	IFS	FS		uppercase	uppercase
29	1D	1101	IGS	GS	8		= ^
30	1E	1110	IRS	RS			
31	1F	1111	IUS	US		Ⓒ (EOT)	Ⓒ (EOT)
32	20	0010 0000	DS	space		@	t
33	21	0001	SOS	!	EOT		
34	22	0010	FS	"	D (even parity)		
35	23	0011		#	D (odd parity)	/	x
36	24	0100	BYP	$	S (even parity)		
37	25	0101	LF	%	S (odd parity)	s	n
38	26	0110	ETB	&		t	u
39	27	0111	ESC	'			
40	28	1000		(			
41	29	1001		)		u	e
42	2A	1010	SM	*		v	d
43	2B	1011	CU2	+	T		
44	2C	1100		,		w	k
45	2D	1101	ENQ	-	4		
46	2E	1110	ACK	.			
47	2F	1111	BEL	/		x	c
48	30	0011 0000		0	forms feed		
49	31	0001		1	forms feed	y	l
50	32	0010	SYN	2		z	h
51	33	0011		3	L		
52	34	0100	PN	4			
53	35	0101	RS	5	,		
54	36	0110	UC	6			

Decimal	Hex	Binary	EBCDIC	ASCII (see note)	Eight-bit data inter-change	PTTC/EBCD	PTTC/correspondence
55	37	0011 0111	EOT	7		Ⓢ (SOA),comma	b
56	38	1000		8			
57	39	1001		9			
58	3A	1010		:	\ (even parity)		
59	3B	1011	CU3	;	\ (odd parity)	index	index
60	3C	1100	DC4	<	< (even parity)		
61	3D	1101	NAK	=	< (odd parity)	Ⓑ (EOB)	
62	3E	1110		>			
63	3F	1111	SUB	?			
64	40	0100 0000	space	@		Ⓝ ,-	!
65	41	0001		A	EOA		
66	42	0010		B	B (even parity)		
67	43	0011		C	B (odd parity)	i	m
68	44	0100		D	" (even parity)		
69	45	0101		E	" (odd parity)	k	
70	46	0110		F		l	v
71	47	0111		G			
72	48	1000		H			
73	49	1001		I		m	'
74	4A	1010	¢	J		n	r
75	4B	1011	.	K	R		
76	4C	1100	<	L		o	i
77	4D	1101	(	M	2		
78	4E	1110	+	N			
79	4F	1111	]	O		p	a
80	50	0101 0000	&	P	line feed		
81	51	0001		Q	line feed	q	o
82	52	0010		R		r	s
83	53	0011		S	J		
84	54	0100		T			
85	55	0101		U	*		
86	56	0110		V			
87	57	0111		W		$	w
88	58	1000		X			
89	59	1001		Y			
90	5A	1010	!	Z	Z (even parity)		
91	5B	1011	$	[	Z (odd parity)	CRLF	CRLF
92	5C	1100	*	\	: (even parity)		
93	5D	1101	)	]	: (odd parity)	backspace	backspace
94	5E	1110	;	Λ		idle	idle
95	5F	1111	¬	—			
96	60	0110 0000	-		ACK		
97	61	0001	/	a		&	j
98	62	0010		b		a	g
99	63	0011		c	F		
100	64	0100		d		b	
101	65	0101		e	&		
102	66	0110		f			
103	67	0111		g		c	f
104	68	1000		h		d	p
105	69	1001		i			
106	6A	1010	¦	J	V (even parity)		
107	6B	1011	,	k	V (odd parity)	e	
108	6C	1100	%	l	6 (even parity)		
109	6D	1101	—	m	6 (odd parity)	f	q
110	6E	1110	>	n		g	comma
111	6F	1111	?	o			
112	70	0111 0000	p			h	/
113	71	0001	q		shift out		
114	72	0010	r		N (even parity)		

Decimal	Hex	Binary	EBCDIC	ASCII (see note)	Eight-bit data inter-change	PTTC/EBCD	PTTC/ correspondence
115	73	0011		s	N (odd parity)	i	y
116	74	0100		t	. (even parity)		
117	75	0111 0101		u	. (odd parity)		
118	76	0110		v		Ⓨ ,period	
119	77	0111		w			
120	78	1000		x			
121	79	1001		v			
122	7A	1010	:	z		horiz tab	tab
123	7B	1011	#	{	↑		
124	7C	1100	@			lowercase	lowercase
125	7D	1101	'	}	>		
126	7E	1110	=	~			
127	7F	1111	''	DEL		delete	
128	80	1000 0000					
129	81	0001	a		SOM	space	space
130	82	0010	b		A (even parity)	=	±,[
131	83	0011	c		A (odd parity)		
132	84	0100	d		! (even parity)	<	@
133	85	0101	e		! (odd parity		
134	86	0110	f				#
135	87	0111	g			;	#
136	88	1000	h		X-ON	:	%
137	89	1001	i				
138	8A	1010					
139	8B	1011			Q	%	&
140	8C	1100					
141	8D	1101			1	'	¢
142	8E	1110				>	*
143	8F	1111					
144	90	1001 0000			horiz tab	*	$
145	91	0001	j		horiz tab		
146	92	0010	k				
147	93	0011	l		I	(	)
148	94	0100	m				
149	95	0101	n		)	)	Z
150	96	0110	o			Ⓓ (EOA),''	(
151	97	0111	p				
152	98	1000	q				
153	99	1001	r				
154	9A	1010			Y (even parity)		
155	9B	1011			Y (odd parity)		
156	9C	1100			9 (even parity)	uppercase	uppercase
157	9D	1101			9 (odd parity)		
158	9E	1110					
159	9F	1111				Ⓒ (EOT)	Ⓒ (EOT)
160	A0	1010 0000			WRU (even)	¢	T
161	A1	0001	~		WRU (odd)		
162	A2	0010	s				
163	A3	0011	t		E	?	X
164	A4	0100	u				
165	A5	0101	v		%	S	N
166	A6	0110	w			T	U
167	A7	0111	x				
168	A8	1000	y				
169	A9	1001	z			U	E
170	AA	1010			U (even parity)	V	D
171	AB	1011			U (odd parity)		
172	AC	1100			5 (even parity)	W	K

Decimal	Hex	Binary	EBCDIC	ASCII (see note)	Eight-bit data interchange	PTTC/EBCD	PTTC/ correspondence
173	AD	1101			5 (odd parity)		
174	AE	1110					
175	AF	1111				X	C
176	B0	1011 0000					
177	B1	0001			return	Y	L
178	B2	0010			M (even parity)	Z	H
179	B3	1011 0011			M (odd parity)		
180	B4	0100			- (even parity)		
181	B5	0101			- (odd parity)		
182	B6	0110					
183	B7	0111				Ⓢ (SOA), |	B
184	B8	1000					
185	B9	1001					
186	BA	1010					
187	BB	1011			]	index	index
188	BC	1100					
189	BD	1101			=	Ⓑ (EOB)	
190	BE	1110					
191	BF	1111					
192	C0	1100 0000	{		EOM (even)	Ⓝ ,—	
193	C1	0001	A		EOM (odd)		
194	C2	0010	B				
195	C3	0011	C		C	J	M
196	C4	0100	D				
197	C5	0101	E		#	K	
198	C6	0110	F			L	V
199	C7	0111	G				
200	C8	1000	H				
201	C9	1001	I		X-OFF	M	''
202	CA	1010			S (even parity)	N	R
203	CB	1011			S (odd parity)		
204	CC	1100	ʃ		3 (even parity)	O	I
205	CD	1101			3 (odd parity)		
206	CE	1110	ᵀ				
207	CF	1111				P	A
208	D0	1101 0000	}				
209	D1	0001	J		vertical tab	Q	O
210	D2	0010	K		K (even parity)	R	S
211	D3	0011	L		K (odd parity)		
212	D4	0100	M		+ (even parity)		
213	D5	0101	N		+ (odd parity)		
214	D6	0110	O				
215	D7	0111	P			!	W
216	D8	1000	Q				
217	D9	1001	R				
218	DA	1010					
219	DB	1011			[	CRLF	CRLF
220	DC	1100					
221	DD	1101			;	backspace	backspace
222	DE	1110				idle	idle
223	DF	1111			PAD		
224	E0	1110 0000	\				
225	E1	0001			bell	+	J
226	E2	0010	S		G (even parity)	A	G
227	E3	0011	T		G (odd parity)		
228	E4	0100	U		, (even parity)	B	+
229	E5	0101	V		, (odd parity)		
230	E6	0110	W				

Decimal	Hex	Binary	EBCDIC	ASCII (see note)	Eight-bit data interchange	PTTC/EBCD	PTTC/correspondence
231	E7	0111	X			C	F
232	E8	1000	Y			D	P
233	E9	1001	Z				
234	EA	1010					
235	EB	1011			W	E	
236	EC	1100					
237	ED	1101			7	F	Q
238	EE	1110				G	comma
239	EF	1111					
240	F0	1111 0000	0		shift in (even)	H	?
241	F1	0001	1		shift in (odd)		
242	F2	0010	2				
243	F3	0011	3		O	I	Y
244	F4	0100	4				
245	F5	0101	5		/		
246	F6	0110	6			Ⓨ , ⌐	—
247	F7	0111	7				
248	F8	1000	8				
249	F9	1001	9				
250	FA	1010	LVM		⇐ (even parity)	horiz tab	tab
251	FB	1011			⇐ (odd parity)		
252	FC	1100			? (even parity)	lowercase	lowercase
253	FD	1101			? (odd parity)		
254	FE	1110			delete	delete	
255	FF	1111			rub out		

Note: When used with the BSCA, the software must maintain parity in bits 0—7 of each byte.

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IBM Series/1 Binary Synchronous Communications
Feature Description
Order No. GA34-0244-0

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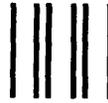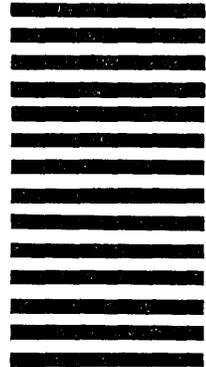
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